


SOLE INVENTOR

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**APPLICATION FOR
UNITED STATES LETTERS PATENT**

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that I, Francesco PIAZZI, a citizen of Switzerland,
residing at Via Alla Chiesa, CH-6928, in the City of Bioggio, in the Country of
Switzerland, have invented a new and useful RF RECEIVER WITH POWER
OFF CONTROL, of which the following is a specification.

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FO600T" E65E2650

CROSS REFERENCE TO RELATED APPLICATIONS

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This application claims the priority of European patent application 00810933.2, filed October 10, 2000, the disclosure of which is incorporated herein by reference in its entirety.

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BACKGROUND OF THE INVENTION

The invention relates to a radio frequency receiver according to the preamble of the independent claim.

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It has been known to provide electronic circuits with power save or control units for switching the circuits off when they are not used. When switching the circuits off, it may be required or desirable that their settings are saved. E.g. when switching a TV off by a remote control, its current loudness settings should be preserved. For this purpose, a control voltage controlling the loudness is stored in a digital memory, from where it is fed to an D/A-converter when the device is switched back on. This, however, requires additional circuitry.

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Furthermore, it has been known to preserve energy in radio frequency receivers by switching the receiver section on and off, in particular in receivers of digital data with a known time structure. In such receivers, the settings of the receiver section, e.g. the control voltage of a VCO in a PLL, are usually lost during power-off periods. When these components are switched back on, some time passes before the settings have been re-established.

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BRIEF SUMMARY OF THE INVENTION

5 Hence, the problem to be solved by the present invention is to provide an RF receiver of the type mentioned above that maintains its settings while being switched off without requiring additional complicated circuitry.

10 Now, in order to implement these and still further objects of the invention, which will become more readily apparent as the description proceeds, the radio receiver is manifested by the features that it comprises circuit elements a setting of which is controlled by at least one control voltage, a control unit for switching off the
15 circuit elements during power-off periods, and a storage for storing the control voltage while the circuit elements are switched off, wherein the storage comprises a storage capacitor storing the control voltage.

20 In a further aspect of the invention, the radio frequency receiver comprises a frequency downconverter for downconverting an incoming signal to an intermediate frequency, an oscillator circuit being connected to the downconverter, a frequency of said oscillator being controlled by a control voltage, a control unit for switching
25 off the oscillator during power-off periods, and a capacitor for storing the control voltage while the oscillator is switched off.

30 To store the setting, the corresponding control voltage is stored in a storage capacitor. This obviates the need for providing a digital memory and a D/A-converter. Since the control voltage needs not be converted to digital information and back, circuitry remains simple and power consumption is reduced.

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For a reliable storage of the control voltage, a discharge time of the capacitor during switch-off should be much larger than a typical switch-off time.

To increase storage time, an electronic switch
5 can be provided for disconnecting the capacitor from at least part of the circuit elements while they are switched off. Alternatively or in addition to that, an active hold circuit can be used for maintaining the voltage over the capacitor.

The technology described here is particularly
10 useful for RF receivers. When part of an RF receiver is switched off for reducing power consumption or during periods of high electronic noise from a radio transmitter in the same appliance, its settings can be maintained using capacitive storage.

15 In particular, RF receivers usually comprise down-converters, where the incoming signal is mixed to a reference frequency. The reference frequency is usually generated by a VCO in a PLL. If such a circuit is switched off and back on, it requires some time to regain stable
20 reference frequency unless the voltage controlling the VCO is stored.

BRIEF DESCRIPTION OF THE DRAWINGS

25 The invention will be better understood and objects other than those set forth above will become apparent when consideration is given to the following detailed description thereof. Such description makes reference to the annexed drawings, wherein:

30 Fig. 1 shows a circuit diagram of an RF receiver,
Fig. 2 part of the automatic gain control circuit, and
Fig. 3 part of the PLL circuit.

DETAILED DESCRIPTION OF THE INVENTION

5 receiver shown in Fig. 1. The receiver shown here is used for receiving the signal of GPS satellites at 1575.42 MHz, but the same technique can be applied to other type of radio receivers, in particular for digital signals.

10 The receiver comprises an antenna 1 with low noise amplifier 2 and an input filter 3. The signal from input filter 3 is fed to a frequency mixer 4, which mixes the carrier at 1575.42 MHz with a frequency of 1554.96 MHz to generate a downconverted first IF signal at 20.46 MHz. The first IF signal is filtered in a first IF filter 5 and fed to
15 a second mixer 6, where it is mixed with a frequency of 16.368 MHz to generate a second downconverted IF signal at 4.092 MHz. The second IF signal is fed through a second IF filter 7 and to a adjustable amplifier 8. The output of adjustable amplifier 9 is fed to an A/D-converter 9 which
20 generates a digital value of two bits SGN and MAG giving the sign and magnitude of the signal. The magnitude bit is analyzed by an adjustable gain control (AGC) 10 to set the gain of adjustable amplifier 8.

25 The design of AGC 10 is shown in Fig. 2. It comprises a switch control unit 20 controlling a switch 21. In a first state, switch 21 connects a capacitor C1 via a current source 22 to the positive supply voltage Vdd. In a second state, switch 21 connects capacitor C1 via a current source 23 to the negative supply voltage or ground. In a
30 thirds state, switch 23 is in high impedance state. The voltage U1 over C1 is fed as a control voltage to the high impedance input of a buffer 24, the output of which controls

amplifier 8, wherein a lower voltage U1 corresponds to a higher amplification in amplifier 8.

In normal operation, if MAG is 1, switch 21 is in its first state and, if MAG is 0, switch 21 is in its second state, i.e. the voltage over capacitor C1 is proportional to the average value of MAG. If the average value of MAG is large, voltage U1 increases, thereby decreasing the amplification of adjustable amplifier 8 and vice versa. The gain loop is adjusted such that it tries to hold MAG at an average value of 0.33, thereby holding the average signal strength at a desired value.

The circuit of Fig. 1 further comprises a Quartz oscillator 11 operating at 16.368 MHz. It generates the reference frequency for second mixer 6. Furthermore, it provides a frequency base for a PLL. The PLL comprises a phase and frequency comparator 12 for comparing the Quartz oscillator frequency divided by 16 to the PLL's frequency divided by 1520. The output of comparator 12 is fed to a low pass filter comprising storage capacitors C2, C3, the voltage U2 over which is the control voltage for the resonance frequency of a tank circuit 13 of a VCO 14. By this arrangement, the VCO's frequency is kept at 1554.96 MHz, the reference frequency for first mixer 4.

The design of the part of the PLL that drives capacitors C2, C3 is shown in Fig. 3. It comprises a switch control unit 26 controlling a switch 27. In a first state, switch 27 connects capacitors C2, C3 via a current source 29 to the positive supply voltage Vdd. In a second state, switch 27 connects capacitors C2, C3 via a current source 30 to the negative supply voltage or ground. In a third state, switch 27 is in high impedance state. If the comparator finds that the VCO's frequency is too low, switch 27 is primarily set to its first state, thereby increasing voltage U2 over the

capacitors, while, if the VCO's frequency is too high and for decreasing voltage U2, switch 27 is primarily in its second state.

The circuit of Fig. 1 comprises a control or power save unit 15. The purpose of this power save unit is to temporarily switch off the circuits of the RF receiver for conservation of power. The position and length of the switch-off periods can e.g. be selected according to a known temporal structure of the incoming signal or according to requirements of the user of the RF receiver.

Power save unit 15 switches off power supply to mixers 4, 6, amplifiers 2, 8, ADC 9 and AGC 10, as well as to the PLL (comparator 12, VCO 14 and frequency dividers) by issuing a control signal PWR SAVE. Typical power-off periods may e.g. have a duration between 1 ms and several seconds.

After a power-off period, power to the circuits of the RF receiver is switched back on and the RF receiver should become operational quickly. Without special provisions, the start-up time of the receiver would be limited by the time it takes for the circuit to re-establish its dynamic settings. These settings are the amplification of adjustable amplifier 8 as well as the frequency of the PLL. To reduce the start-up time, the circuit of Fig. 1 is designed to store these settings as control voltages U1, U2 over the capacitors C1 and C2 or C3. While power is off, the load impedance offered by the circuits to these capacitors is high enough to make the discharge time of the capacitors much longer than a typical power-off period. A typical power-off period is e.g. limited by a few seconds, while the discharge time is e.g. 100 times as large.

It must be noted that the capacitors C1, C2 and C3 serve two purposes. First they act as low pass filters or integrators in their corresponding feed-back loops (ACG and

PLL), second they store the setting of the loop during power-off.

To achieve high discharge times, switches 21 and 27 are both set to their third, high impedance state while the signal PWR SAVE indicates that the circuit is switched off.

To reach even higher discharge times, the capacities of the capacitors can be increased where possible. In addition or alternatively to this, active hold circuits can be used to maintain the voltage of the capacitors during power-off periods. In such a circuit, the storage capacitor can e.g. be arranged in the negative feedback loop between the amplifier output and its inverting input.

The LNA 2, the frequency mixers 4, 6, the filters 5, 7, the amplifier 8 and the AGC 10 form the analogue section of the receiver of Fig. 1. In the shown embodiment, the settings of this section are stored during power-off periods by saving the control voltages for the amplifier 8 and the VCO.

By storing the control voltages in the capacitors, the circuit can be switched back on quickly because its settings are maintained.

The principle described here can be used in other electronic circuits having settings that can be controlled by control voltages. In such circuits, the control voltages can be stored in suitable capacitors while power is shut down. The technique shown here is especially suited for PLL circuits in any application or for storing the amplification setting or setpoint of an adjustable RF or LF amplifier. It can also be used for storing the settings of any feedback loops.

In the embodiment described above, power save unit 15 is controlled automatically, i.e. the time and

duration of the switch-off periods are not directly determined by the user. However, power save unit 15 could also be controlled by the user directly.

- 5 While there are shown and described presently preferred embodiments of the invention, it is to be distinctly understood that the invention is not limited thereto but may be otherwise variously embodied and practised within the scope of the following claims.